

UPPER-BOUND CALCULATION FOR PLACED CIRCUIT DESIGN PERFORMANCE

ABSTRACT

Within a computer automated tool, a method (400) of estimating an upper-bound of an operational frequency of at least a portion of a placed circuit design can include identifying (405) a clock source within the placed circuit design, wherein the clock source is associated with a clock domain, and determining (410) an initial routing of the clock domain. The method also can include determining (420) a minimum path slack corresponding to each connection of the clock domain. Connections of the clock domain which have a lowest minimum path slack can be marked (430). One or more marked connections which are not routed in delay mode can be identified and routed in delay mode (455) allowing sharing of routing resources by different nets.